Claims:

1. A system to initiate, by a host, an event in a first device, the system comprising:

a signal line to communicate a plurality of data values between a host and one or more second devices; and

a tap line to communicate said plurality of data values between said signal line and said first device;

wherein said event is initiated upon detection, by said first device, of a predetermined sequence of data values on the tap line.

2. The system of claim 1, wherein the event comprises a switching from a communication path between the first device and a third device and a communication path between the signal line and the third device.

3. The system of claim 1, wherein the event comprises a switching from a communication path between a signal line and a third device and a communication path between the first device and the third device.

4. The system of claim 1, wherein the host is a processor.

5. The system of claim 1, wherein the first device is a logic device.

6. The system of claim 1, wherein each of the one or more second devices is a memory device.

7. The system of claim 1, wherein the third device is a memory device.

8. The system of claim 1, wherein the host is a microprocessor chipset, the first device is a Field Programmable Gate Array (FPGA), each of the one or more second devices is a Dual In-line Memory Module (DIMM), and the third device is Synchronous Dynamic Random Access Memory (SDRAM).

9. The system of claim 1, wherein each of the plurality of data values represents a memory location within any of the plurality of second memory devices.

10. The system of claim 9, wherein utilization of a data value provides a call to the represented memory location.

11. A method to initiate, by a host, an event in a first device comprising:

communicating, by a signal line, a plurality of data values between a host and one or more second devices;

communicating, by a tap line, said plurality of data values between said signal line and said first device; and

initiating said event upon detection by said first device of a predetermined sequence of data values on the tap line.

12. The method of claim 11, wherein the event comprises a switching from a communication path between the first device and a third device and a communication path between the signal line and the third device.

13. The method of claim 11, wherein the event comprises a switching from a communication path between a signal line and a third device and a communication path between the first device and the third device.

14. The method of claim 11, wherein the host is a processor.

15. The method of claim 11, wherein the first device is a logic device.

16. The method of claim 11, wherein each of the one or more second devices is a memory device.

17. The method of claim 11, wherein the third device is a memory device.

18. The method of claim 11, wherein the host is a microprocessor chipset, the first device is a Field Programmable Gate Array (FPGA), each of the one or more second devices is a Dual In-line Memory Module (DIMM), and the third device is Synchronous Dynamic Random Access Memory (SDRAM).

19. The method of claim 11, wherein each of the plurality of data values represents a memory location within any of the plurality of second memory devices.

20. The method of claim 19, wherein utilization of a data value provides a call to the represented memory location.

21. A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor to initiate, by a host, an event in a first device comprising:

communicating, by a signal line, a plurality of data values between a host and one or more second devices;

communicating, by a tap line, said plurality of data values between said signal line and said first device; and

initiating said event upon detection by said first device of a predetermined sequence of data values on the tap line.

22. The set of instructions of claim 21, wherein the event comprises a switching from a communication path between the first device and a third device and a communication path between the signal line and the third device.

23. The set of instructions of claim 21, wherein the event comprises a switching from a communication path between a signal line and a third device and a communication path between the first device and the third device.

24. The set of instructions of claim 21, wherein the host is a processor.

25. The set of instructions of claim 21, wherein the first device is a logic device.

26. The set of instructions of claim 21, wherein each of the one or more second devices is a memory device.

27. The set of instructions of claim 21, wherein the third device is a memory device.

28. The set of instructions of claim 21, wherein the host is a microprocessor chipset, the first device is a Field Programmable Gate Array (FPGA), each of the one or more second devices is a Dual In-line Memory Module (DIMM), and the third device is Synchronous Dynamic Random Access Memory (SDRAM).

29. The set of instructions of claim 21, wherein each of the plurality of data values represents a memory location within any of the plurality of second memory devices.

30. The set of instructions of claim 29, wherein utilization of a data value provides a call to the represented memory location.